

CLAIMS

What is claimed is:

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Sub B7
1. A logic device, comprising:
a plurality of interconnecting carbon nanotube devices, wherein said
interconnecting carbon nanotube devices comprise a plurality of electrically
connected carbon nanotubes on one or more levels of a substrate, and wherein
said carbon nanotubes are formed within at least one nanosized catalyst
retaining structure in said substrate.
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 2. The logic device of Claim 1, further comprising one or more
electrical bond pads coupled to the plurality of carbon nanotube devices and
configured to provide external electrical connections to the logic device.
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 3. The logic device of Claim 1, wherein said plurality of
interconnecting carbon nanotube devices is electrically connected via patterned
electrically conducting films.
 - 20 4. The logic device of Claim 1, wherein said plurality of
interconnecting carbon nanotube devices is electrically connected via patterned
electrically conducting carbon nanotubes.
 - 25 5. The logic device of Claim 1, wherein said plurality of
interconnecting carbon nanotube devices are electrically connected via a
combination of patterned electrically conducting films and patterned electrically
conducting carbon nanotubes.
 - 30 6. The logic device of Claim 3, wherein said patterned electrically
conducting films are metallic films.
 7. The logic device of Claim 1, wherein a plurality of carbon nanotube
devices are formed on a single carbon nanotube and wherein said plurality of

carbon nanotube devices are electrically isolated by non-conducting segments of said single carbon nanotube.

5 8. The logic device of Claim 2, wherein said electrical bond pads comprise metallic bond pads.

 9. The logic device of Claim 8, wherein said metallic bond pads are lithographically fabricated.

10 10. The logic device of Claim 1, wherein said device is fabricated on a doped silicon substrate.

 11. The logic device of Claim 1, wherein said device is fabricated on an aluminum substrate.

15 12. The logic device of Claim 1, wherein said device is fabricated on a substrate suitable for electrochemical etching.

 13. The logic device of Claim 12, wherein said substrate further comprises metal interconnects coupled to said carbon nanotube devices.

 14. The logic device of Claim 12, wherein said substrate comprises layers of doped crystalline silicon and patterned metal interconnects.

25 15. The logic device of Claim 12, wherein said substrate is fabricated by stacking of deposited metal lines and epitaxially grown or deposited silicon layer, followed by ion implantation and recrystallization of the silicon.

 16. The logic device of Claim 12, wherein said substrate further comprises a plurality of layers bonded together.

30 17. The logic device of Claim 11, wherein said substrate further comprises layers of aluminum and patterned metal interconnects fabricated by stacking deposited metal lines and recrystallized deposited aluminum.

18. A method of fabricating a carbon nanotube device, comprising the steps of:

fabricating a template of nanosized catalyst retaining structures within a substrate;

5 depositing catalyst within said nanosized catalyst retaining structures; and
synthesizing carbon nanotubes that conform to said template of said nanosized catalyst retaining structures.

10 19. The method of Claim 18, wherein said template bounds a pattern of said carbon nanotube devices.

20. The method of Claim 18, wherein said template bounds a length of said carbon nanotube devices.

15 21. The method of Claim 18, wherein said template bounds a vertical profile of said carbon nanotube devices.

20 22. The method of Claim 18, wherein said nanosized catalyst retaining structures comprise uniform holes used to synthesize vertical carbon nanotube interconnects and non-uniform holes used to synthesize carbon nanotube devices.

25 23. The method of Claim 18, further comprising the step of interconnecting carbon nanotube devices with electrically conducting interconnects to form logic devices.

24. The method of Claim 18, wherein said template is fabricated by etching said substrate at specified locations.

30 25. The method of Claim 24, wherein said specified locations are patterned using lithographic techniques.

26. The method of Claim 18, wherein fabricating said template comprises placing of an impurity, local defect, stress, or optical energy to initiate formation of said nanosized catalyst retaining structures.

5 27. The method of Claim 22, wherein said non-uniform holes have discontinuities in diameter along a vertical axis of said holes.

28. The method of Claim 27, wherein said template is generated by using electrochemical etching or photo-electrochemical etching.

10 29. The method of Claim 28, wherein said electrochemical etching process is varied by process parameters selected from the group consisting of current density, concentration of the etchant, doping of the silicon substrate, and luminescence.

15 30. The method of Claim 29, wherein dynamic control of a diameter of a hole of said templates along a vertical axis is achieved by controlling said process parameters as a function of depth of penetration, etching rate and etching time.

20 31. The method of Claim 29, wherein dynamic control of a diameter of a hole of said templates along a vertical axis is achieved by controlling a current flux as a function of time.

25 32. The method of Claim 29, wherein said electrochemical etching of a doped silicon substrate is achieved with a diluted HF acid and current densities of 10 mA/cm².

30 33. The method of Claim 32, wherein said electrochemical etching is configured to produce a cylindrical template with a bulge or an hour-glass shaped template.

34. The method of Claim 32, wherein said electrochemical etching is configured to produce a cylindrical template with a diameter between 1 and 50 nm.

5 35. The method of Claim 28, wherein said substrate is an aluminum substrate, and wherein said electrochemical etching process is varied by process parameters selected from the group consisting of current density and concentration of the etchant.

10 36. The method of Claim 35, wherein dynamic control of a diameter of a hole of said templates along a vertical axis is achieved by controlling said process parameters as a function of depth of penetration, etching rate and etching time.

15 37. The method of Claim 35, wherein dynamic control of a diameter of a hole of said templates along a vertical axis is achieved by controlling a current flux as a function of time.

20 38. The method of Claim 35, wherein said electrochemical etching of a doped silicon substrate is achieved with a diluted HF acid and current densities of 10 mA/cm².

25 39. The method of Claim 35, wherein said electrochemical etching is configured to produce a cylindrical template with a bulge or an hour-glass shaped template.

30 40. The method of Claim 35, wherein said electrochemical etching is configured to produce a cylindrical template with a diameter between 1 and 50 nm.

41. The method of Claim 18, wherein catalyst comprises a metal catalyst.

42. The method of Claim 41, wherein said metal catalyst is selected from the group consisting of Fe, Ni, and Co.

5 43. The method of Claim 41, wherein said catalyst is deposited using chemical deposition or electro-deposition.

10 44. The method of Claim 41, wherein said deposition of said metal catalyst is achieved concurrently with said fabrication of said template by incorporating a metal catalyst in an electrochemical etching solution.

45. The method of Claim 44, wherein said etching solution comprises HF with traces of iron to introduce catalytic metal into said etching solution.

15 46. The method of Claim 18, wherein synthesizing said nanotubes comprises thermal deposition of hydrocarbides using a CVD process.

47. A method for manufacturing an array of transistors, comprising:
growing aligned carbon nanotubes within a catalyst retaining
template; and

introducing one or more discontinuities within a structure of said
carbon nanotubes, wherein said discontinuities are conductivity discontinuities
along a vertical axis of said carbon nanotubes, wherein if one discontinuity is
introduced a diode is formed and if two discontinuities is introduced a transistor is
formed.

48. The method of Claim 47, wherein said discontinuities comprise
variations in a diameter of said carbon nanotubes or impurities in said carbon
nanotube.

49. The method of Claim 48, wherein said variations in said diameter
of said carbon nanotubes are achieved by varying an electrochemical etch
process.

50. The method of Claim 47, wherein said catalyst retaining structure
is formed on a substrate.

51. The method of Claim 47, wherein said at least two discontinuities
comprise pentagon-heptagon pairs.

52. The method of Claim 47, wherein more than at least two
discontinuities are introduced within said structure of said carbon nanotube to
produce one or more carbon nanotube transistors along said vertical axis.

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53. A carbon nanotube transistor, comprising:
a carbon nanotube with at least two defects in said carbon
nanotube, and wherein said defects divide said carbon nanotube into three
regions with differing conductivities.

54. The carbon nanotube transistor of Claim 53, wherein said defects
comprise variations in a diameter of said carbon nanotubes.

55. The carbon nanotube transistor of Claim 54, wherein said
variations in said diameter of said carbon nanotubes are achieved by varying an
electrochemical etch process.

56. The carbon nanotube transistor of Claim 53, wherein said catalyst
retaining structure is formed within a substrate.

57. The carbon nanotube transistor of Claim 53, wherein said at least
two discontinuities comprise pentagon-heptagon pairs.

58. The carbon nanotube transistor of Claim 53, wherein more than
two discontinuities are introduced within said structure of said carbon nanotube to
produce a plurality of carbon nanotube transistors along said vertical axis.

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59. A logic device, comprising:
a substrate;
a layer of insulating material in which at least one catalyst retaining
structure is formed;

5 at least one carbon nanotube formed within said catalyst retaining
structure, wherein said at least one carbon nanotube has at least two defects in
said carbon nanotube, and wherein said defects divide said carbon nanotube into
at least three regions with differing conductivities.

10 60. The logic device of Claim 59, wherein said defects comprise
variations in a diameter of said carbon nanotubes;

15 61. The logic device of Claim 60, wherein said variations in said
diameter of said carbon nanotubes are achieved by varying an electrochemical
etch process.

62. The logic device of Claim 59, wherein said catalyst retaining
structure is formed on a substrate.

20 63. The logic device of Claim 59, wherein said at least two
discontinuities comprise pentagon-heptagon pairs.

25 64. The logic device of Claim 59, wherein more than two
discontinuities are introduced within said structure of said carbon nanotubes to
produce a plurality of carbon nanotube transistors along said vertical axis.